This document is a preprint of: S. Krone and G. Fettweis, "Energy-Efficient A/D Conversion in Wideband Communications Receivers," in Proceedings of IEEE Vehicular Technology Conference (VTC Fall 2011), San Francisco, USA, Sep 2011. DOI:10.1109/VETECF.2011.6093142

# Energy-Efficient A/D Conversion in Wideband Communications Receivers

Stefan Krone and Gerhard Fettweis
Vodafone Chair Mobile Communications Systems
Technische Universität Dresden, 01062 Dresden, Germany
E-mail: {stefan.krone, fettweis}@ifn.et.tu-dresden.de

***Abstract*—The energy consumption of wideband communications receivers depends highly on the parametrization of the A/D conversion stage. The design of energy-efficient receivers requires an optimal parametrization. This paper investigates the power dissipation of state-of-the-art A/D converters and studies the optimal parametrization from an information theoretic perspective. The results show that a large sampling rate and very low quantization resolution will usually be most energy-efficient.**

## I. Introduction

A major challenge for the design of energy-efficient wideband communications receivers is the analog-to-digital (A/D) conversion. When the sampling rate reaches several GHz, the power dissipation of modern A/D converters is on the order of Watts and dominates the receiver energy consumption. The power dissipation can be reduced when restricting to low quantization resolution. This affects, however, the maximum system throughput when the resolution gets too low.

This paper analyzes the optimal parametrization of A/D converters in wideband communications receivers to minimize the energy consumption for a target system throughput. The analysis builds on analytical expressions that relate the power dissipation to the sampling rate and quantization resolution. Moreover, it builds on a numerical computation of the maximum spectral efficiency, i.e. the channel capacity, using the approach proposed in [1], but extended to complex-valued transmission. The optimal parameterization trades-off the required sampling rate and quantization resolution to achieve a target system throughput under a transmit power constraint. This is different from the approach in [2], as it does not minimize the overall power dissipation including the transmit power. Instead, a fixed average transmit power is assumed to be available. Further differences are that the channel capacity is not approximated but calculated exactly, and that state-of-the-art ADCs are considered in addition to the sample-and-hold capacitor noise limit. The result confirms the principle observation in [2]: A/D converters with very low quantization resolution but large sampling rate are typically optimal to minimize the energy consumption of wideband communications receivers.

The paper is organized as follows: Section II introduces the system model. The maximum spectral efficiency and its computation are discussed in Section III. Section IV studies the power dissipation of A/D converters, and Section VI analyzes their optimal parametrization to maximize the energy efficiency. Conclusions are finally drawn in Section V.

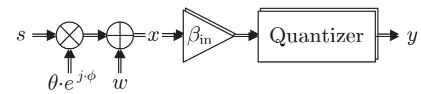


Fig. 1: System model: LOS channel with quantization at the receiver.

## II. System Model

Consider a wideband system that shall be designed for line-of-sight (LOS) channels without multi-path propagation. The sampling rate and the quantization resolution at the receiver are determined by the A/D converters. Sampling at symbol rate will be considered. Fig. 1 shows the system model. It reads

$$y = \mathrm{Q}_M\big(\beta_{\mathrm{in}} \cdot (\theta \cdot e^{j\cdot\phi} \cdot s + w)\big), \tag{1}$$

where $\mathrm{Q}_M(\cdot)$ denotes the quantization with $M$ levels. Uniform quantization is assumed. $s$ denotes the transmitted data symbols, which are complex-valued with zero mean and variance $\sigma_s^2$. An average transmit power constraint applies, which is defined as $\sigma_s^2 = \mathrm{E}_s\{|s|^2\} \leq \Omega_s$, where $\mathrm{E}_s\{\cdot\}$ denotes the expectation over the probability density function (PDF) of $s$. The quantized received samples are complex-valued, too, and denoted as $y$. The sampling and quantization are identical for the in-phase and quadrature-phase. The attenuation $\theta$ and the phase $\phi$ of the LOS channel are static. $w$ models the complex-valued additive white Gaussian noise (AWGN) of the channel, which has zero mean and variance $\sigma_w^2$. A uniform noise power spectral density $\mathcal{N}_0$ implies $\sigma_w^2 = \mathcal{N}_0 \cdot f_s$, where $f_s$ denotes the sampling rate. The signal-to-noise-ratio (SNR) of the channel (at the quantizer input) is thus inverse proportional to the sampling rate:

$$\gamma = \frac{\theta^2 \cdot \sigma_s^2}{\mathcal{N}_0 \cdot f_s}. \tag{2}$$

The receiver amplification $\beta_{\mathrm{in}}$ scales the unquantized received samples, denoted as $x$, to match the quantization input range, which is fixed.

Let $\Xi$ be a target system throughput (in bit/s), which can be expressed as

$$\Xi = \Psi \cdot f_s, \tag{3}$$

where $\Psi$ denotes the required spectral efficiency to achieve the throughput at symbol rate $f_s$. It is obvious that the same throughput can be achieved with different $f_s$ and $\Psi$. However, the latter depends on the SNR and on the quantization resolution at the receiver. The sampling rate and the number of quantization levels can be traded-off to minimize the power

This document is a preprint of: S. Krone and G. Fettweis, “Energy-Efficient A/D Conversion in Wideband Communications Receivers,” in Proceedings of IEEE Vehicular Technology Conference (VTC Fall 2011), San Francisco, USA, Sep 2011. DOI:10.1109/VETECF.2011.6093142

dissipation of the A/D conversion under different channel conditions. The optimal parametrization derives from the maximum spectral efficiency of the channel and from the A/D converter power dissipation, where each is a function of $M$ and $f_s$. These functional dependencies are assessed in the next two sections to derive the optimal parametrization in Section IV.

## III. Maximum Spectral Efficiency

The considered system model is in fact an AWGN channel with $M$-level output quantization as considered in [1], but extended to complex-valued transmission. The maximum spectral efficiency is the capacity of this channel with an optimal calibration of the receiver amplification $\beta_{\text{in}}$. The channel capacity depends on the SNR, and thus inherently on the sampling rate $f_s$, and on $M$.

### A. Derivation

It is known from [1], that the optimal channel input PDF $\mathrm{p}_{\text{real}}(\cdot)$, that achieves the capacity $\mathrm{C}_{\text{real}}$ of an arbitrary real-valued AWGN channel with $M$-level output quantization under the transmit power constraint $\Omega_{\text{real}}$, is discrete and has at most $M+1$ mass points. It is tedious but straight forward to extend this result to complex-valued channels with identical quantization of the in-phase and quadrature-phase. The extension builds on [3, Th. 7.3.1]. It can be shown that the capacity of complex-valued channels is $\mathrm{C}=2\cdot\mathrm{C}_{\text{real}}$, where $\Omega_s=2\cdot\Omega_{\text{real}}$ and the SNR is the same for the real- and the complex-valued channel. The capacity-achieving channel input PDF follows as $\mathrm{p}_s(s)=\mathrm{p}_{\text{real}}\big(\mathfrak{Re}\{e^{-j\cdot\phi}\cdot s\}\big)\cdot\mathrm{p}_{\text{real}}\big(\mathfrak{Im}\{e^{-j\cdot\phi}\cdot s\}\big)$, where $\mathfrak{Re}\{\cdot\}$ and $\mathfrak{Im}\{\cdot\}$ denote the real and imaginary part, respectively. The latter implies that the channel capacity can only be achieved with an equalization of the channel phase at the transmitter or in the analog receiver frontend. Another implication is that the capacity-achieving channel input PDF of the complex-valued channel has at most $(M+1)^2$ mass points. Numerical results indicate that there are never more than $M^2$ mass points. An analytical proof for this observation remains still open.

It should be stressed that the channel capacity is different from the the capacity of discrete memoryless channels considered in [3], as it incorporates a transmit power constraint.

### B. Numerical Computation

The channel capacity and the respective channel inputs can be computed with the Cutting-Plane algorithm [4], as proposed in [1]. The full optimization problem, which includes a maximization over $\beta_{\text{in}}$ when $M>2$, writes

$$\mathrm{C}_{\max} = \max_{\beta_{\text{in}}} \mathrm{C} = \underbrace{\max_{\beta_{\text{in}}} \underbrace{\max_{\mathrm{p}_s(s)} \mathrm{I}(S;Y) \;\;\text{s.t.}\;\; \mathrm{E}_s\{|s|^2\} \le \Omega_s}_{\text{Cutting-Plane algorithm.}}}_{\text{Numerical search.}} \qquad (4)$$

where $\mathrm{I}(S;Y)$ denotes the mutual information [3] between the channel inputs and outputs which results for a given input PDF and a selected $\beta_{\text{in}}$. The computation can be simplified by computing the maximum capacity of the respective real-valued channel and doubling the result, as explained before.

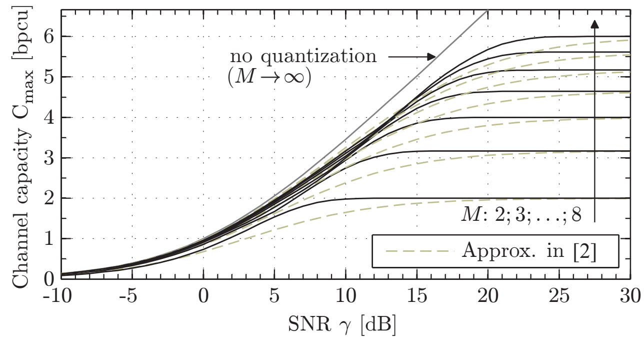


Fig. 2: Maximum channel capacity with optimal $M$-level output quantization.

The channel capacity that could be obtained with non-uniform quantization might in principle be higher than the capacity that assumes uniform quantization. However, the computed results show almost no difference. That is, even when considering non-uniform quantization, the quantizer characteristic that maximizes the channel capacity is virtually uniform, at least for the considered cases with small to quantization resolution, where $M\le 8$.

Fig. 2 shows the computed maximum channel capacity as a function of the SNR and $M$. At low SNR, the channel capacity is dominated by the AWGN. At high SNR, the quantization at the receiver determines the channel capacity. The capacity bound at high SNR is the maximum output entropy with $M$-level quantization, i.e., $\mathrm{C}_{\max} \le 2\cdot\log_2(M)$. The capacity-achieving channel inputs (not shown in this paper) indicate that the the available transmit power is always fully exploited, i.e., $\sigma_s^2=\Omega_s$.

A closed-form approximation of the channel capacity has been considered in [2] to express the functional dependency on the SNR and $M$ analytically. The approximation writes $\mathrm{C}_{\max} \approx \log_2\big((1+\gamma)/(1+\gamma\cdot M^{-2})\big)$. It can be seen in Fig. 2 that the approximation is a rather loose. Therefore, it has not been used for the analysis in this work. However, it appears that the coarse approximation still leads to the same principle result, which suggests that A/D converters with very low quantization resolution are optimal for energy-efficient wideband receivers.

## IV. Power Dissipation of A/D Converters

The power dissipation of A/D converters is closely related to their architecture. Large sampling rates are typically achieved with pipeline, flash or time-interleaved architectures, but only at the price of limited quantization resolution or rather high power dissipation [5].

### A. Sample-and-Hold Capacitor Noise Limit

Technological limits to the power dissipation of different A/D converter architectures have been studied in [6]. The most fundamental limit derives from the sample-and-hold capacitor noise [7]. It is given as

$$\mathrm{P}_{\text{ADC}}=24\cdot k_{\text{B}}\cdot\vartheta\cdot 2^{2\cdot B}\cdot f_{\text{s}}, \qquad (5)$$

where $k_{\text{B}}$ denotes Boltzmann’s constant, and $\vartheta$ is the temperature measured in Kelvin. Comparing this limit to the power

This document is a preprint of: S. Krone and G. Fettweis, “Energy-Efficient A/D Conversion in Wideband Communications Receivers,” in Proceedings of IEEE Vehicular Technology Conference (VTC Fall 2011), San Francisco, USA, Sep 2011. DOI:10.1109/VETECF.2011.6093142

dissipation of state-of-the-art A/D converters it turns out that it hardly reflects todays practical values, which are still several magnitudes above the limit. This holds in particular for A/D converters with high sampling rates.

### B. State-of-the-Art A/D Converters

For the above reason, one track of the analysis in this paper considers an empirical expression of the power dissipation of A/D converters which derives from surveyed data of state-of-the-art designs. The survey is based on the data provided in [8] and further A/D converters that have been published recently in [9]–[18]. The surveyed data covers the most relevant designs with similar characteristics, i.e., A/D converters with at least 1 GHz Nyquist sampling rate that have been fabricated in either CMOS or SiGe BiCMOS technology, and which have been published within the last five years (from 2006 to 2010). 29 A/D converters have been surveyed in total.

Figs. 3 and 4 render the functional dependency of the A/D converter power dissipation on the sampling rate and effective number of bits (ENOB). The ENOB is an effective quantization resolution that accounts for hardware impairments such as circuit noise, sampling clock and aperture jitter, non-linearities and comparator ambiguity. It is typically 0.5 to 1.5 bits below the nominal resolution [5].

For the largest subset of the surveyed A/D converters, where the sampling rates are between 1 and 2 GHz, it can be observed that the power dissipation scales with $2^{2\cdot\mathrm{ENOB}}$. Similarly, when restricting the ENOB to $2\ldots4$ or $4\ldots6$, respectively, the power dissipation appears to scale quadratically with $f_\mathrm{s}$. This implies the following proportional relation of the power dissipation of state-of-the-art A/D converters with sampling rates of 1 GHz and above:

$$\mathrm{P}_\mathrm{ADC} \propto M^2 \cdot f_\mathrm{s}^2, \tag{6}$$

This expression takes into account that the ENOB corresponds to $M = 2^{\mathrm{ENOB}}$ effective (usable) quantization levels. It shows considerable similarity with the power dissipation limit given in (5). The disagreement by the factor $f_\mathrm{s}$ implies that the power dissipation of today's designs is still more increasing with larger sampling rates than the fundamental limit suggests.

Both cases are considered for the analysis in this paper. The power dissipation is therefor generally modeled as

$$\mathcal{P}_\mathrm{ADC} = \mathrm{const.} \cdot M^2 \cdot f_\mathrm{s}^\nu \tag{7}$$

where $\nu = 2$ holds for state-of-the-art A/D converters and $\nu = 1$ for the sample-and-hold capacitor noise limit.

## V. Optimal Parametrization

The analysis is based on the perception that the energy consumption of wideband receivers is either completely dominated by the A/D conversion, or can only be reduced with an optimal A/D converter parametrization while the energy consumption of all other receiver components remains unaffected for the same system throughput. In both cases, an optimal parametrization will minimize the overall energy consumption of the receiver.

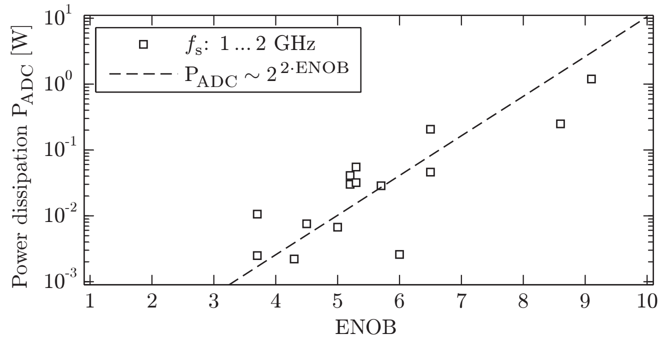


Fig. 3: Power dissipation vs. ENOB of ADCs supporting sampling rates of 1 GHz to 2 GHz.

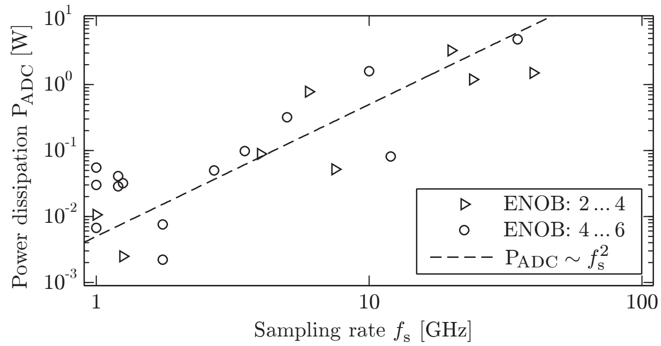


Fig. 4: Power dissipation vs. sampling rate of ADCs with ENOB ranging from 2 to 4 and 4 to 6.

### A. Energy-Efficiency Model

The energy consumption per converted data sample at the receiver is $\mathcal{P}_\mathrm{ADC}/f_\mathrm{s}$. The energy consumption over a time interval $\Delta t$ follows as $(\Delta t \cdot f_\mathrm{s}) \cdot \mathcal{P}_\mathrm{ADC}/f_\mathrm{s}$, where $\Delta t \cdot f_\mathrm{s}$ is the number of samples attained within $\Delta t$. It is obvious that the energy consumption can be minimized by minimizing $\mathcal{P}_\mathrm{ADC}$.

Using (7) and (3), the A/D converter power dissipation can be written as

$$\mathcal{P}_\mathrm{ADC} = \underbrace{\mathcal{P}_\mathrm{ADC,\,ref}}_{\mathrm{const.}\,\cdot\,\Xi^\nu} \cdot \frac{M^2}{\Psi^\nu}. \tag{8}$$

It can be minimized for any target throughput $\Xi$ by optimizing $M$ and $\Psi$. For any choice of $M$, the optimal $\Psi$ that minimizes $\mathcal{P}_\mathrm{ADC}$ is the channel capacity $\mathrm{C}_\mathrm{max}$ which has been considered in Section III. The dependency of $\mathrm{C}_\mathrm{max}$ on the SNR and $M$ can in general be expressed as function

$$\mathrm{F}(M;\gamma) = \mathrm{C}_\mathrm{max}\big|_{M,\,\gamma}. \tag{9}$$

The spectral efficiency that minimizes $M^2/\Psi^\nu$ in (7) follows implicitly as

$$\Psi = \mathrm{F}\left(M;\, \Psi \cdot \frac{\mathcal{E}_\mathrm{bit}}{\mathcal{N}_0}\right), \tag{10}$$

where $\mathcal{E}_\mathrm{bit} = \theta^2 \cdot \Omega_s / \Xi$ denotes the received signal energy per transmitted information bit. The maximum of $\Psi$ follows as a function of $M$ as

$$\Psi_\mathrm{max}(M) \;=\; \max \Psi \quad \text{s.t.} \quad \Psi = \mathrm{F}\left(M,\, \Psi \cdot \frac{\mathcal{E}_\mathrm{bit}}{\mathcal{N}_0}\right), \tag{11}$$

This document is a preprint of: S. Krone and G. Fettweis, “Energy-Efficient A/D Conversion in Wideband Communications Receivers,” in Proceedings of IEEE Vehicular Technology Conference (VTC Fall 2011), San Francisco, USA, Sep 2011. DOI:10.1109/VETECF.2011.6093142

where the right-hand-side of (11) defines the support set of $\Psi$. By minimizing (8) with (11) over $M$, the minimum A/D converter power dissipation finally derives as

$$\mathcal{P}_{\mathrm{ADC,\,min}} = \mathcal{P}_{\mathrm{ADC,\,ref}} \cdot \min_{M} \frac{M^2}{\left(\Psi_{\max}(M)\right)^{\nu}}. \tag{12}$$

Once the function $\mathrm{F}(M;\gamma)$ has been (numerically) computed, a search over $\Psi$ and $M$ can be applied to find the optimal A/D converter parametrization and the minimum power dissipation with (11) as follows:

$$M_{\mathrm{opt}} = \arg\min_{M} \frac{M^2}{\left(\Psi_{\max}(M)\right)^{\nu}}; \tag{13a}$$

$$f_{\mathrm{s,\,opt}} = \frac{\Xi}{\Psi_{\max}(M_{\mathrm{opt}})}; \tag{13b}$$

$$\mathcal{P}_{\mathrm{ADC,\,min}} = \mathcal{P}_{\mathrm{ADC,\,ref}} \cdot \frac{M_{\mathrm{opt}}^2}{\left(\Psi_{\max}(M_{\mathrm{opt}})\right)^{\nu}}. \tag{13c}$$

The spectral efficiency of the channel that results with this parameterization is $\Psi_{\max}(M_{\mathrm{opt}})$. This spectral efficiency is achieved with particular channel inputs and the respective receiver amplification $\beta_{\mathrm{in}}$. Both can be computed with the Cutting-Plane algorithm (i.e. $\arg\max(\cdot)$ in (4)) for the resulting AWGN channel with SNR $\gamma = \Psi_{\max}(M_{\mathrm{opt}}) \cdot \mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0$ and $M_{\mathrm{opt}}$ output levels.

The target system throughput and the channel properties are incorporated in the optimization through

$$\frac{\mathcal{E}_{\mathrm{bit}}}{\mathcal{N}_0} = \frac{\theta^2 \cdot \Omega_s}{\mathcal{N}_0} \cdot \frac{1}{\Xi}, \tag{14}$$

which is in fact a normalization that relates the channel properties to the target throughput. Regardless of the ADC power dissipation and quantization resolution, it is obvious that an arbitrary small $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0$ cannot be achieved. The lower bound is $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0 > 1/\log_2(e) = -1.59\,\mathrm{dB}$, which is the limit when the SNR of the channel approaches zero, while the symbol rate tends to infinity [19, Section 5.2.2]. This bound derives without but also with quantization at the receiver, since the channel capacity is the same at very low SNR (see Fig. 2). The normalization in (14) is used in the next paragraph to discuss the numerical results in general.

### B. Numerical Evaluation

Fig. 5 shows the minimum ADC power dissipation that follows from (7) with (11) as a function of $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0$ and $M$. For reasonably high values of $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0$, it can be observed that a very low quantization resolution is most energy-efficient, which calls for system designs with rather large bandwidth. This confirms the findings in [2].

The observation holds for state-of-the-art ADCs ($\nu = 2$) and is even more pronounced for the sample-and-hold capacitor noise limit ($\nu = 1$). The latter follows from the fact that the power dissipation scales only linearly with the sampling rate such that a large sampling rate and very low quantization resolution become even more favorable.

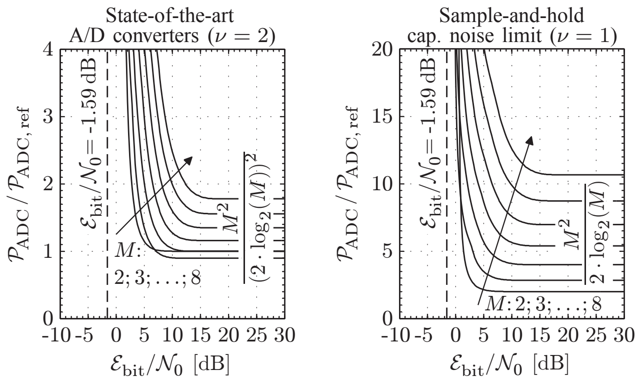


Fig. 5: Minimum A/D converter power dissipation.

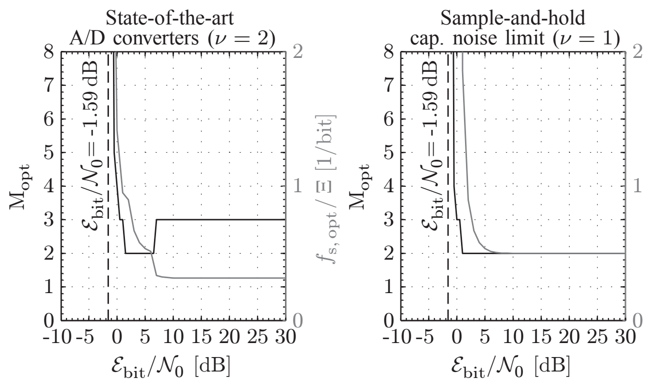


Fig. 6: Optimal A/D converter parametrization.

Fig. 6 compares the optimal quantization resolution and the respective sampling rate (normalized to the target throughput). At medium to high $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0$ it is optimal to restrict to very low quantization resolution, while scaling the sampling rate with the target system throughput. If the target throughput is rather demanding as compared to the available transmit power, reflected in a small $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0$, both the sampling rate and the optimal quantization resolution scale up. As the power dissipation is increasing significantly, it becomes a design trade-off to balance the throughput and the power dissipation. Most practical system designs are typically targeting at medium to high $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0$, as illustrated by the example in the next paragraph.

The reciprocal of $f_s/\Xi$ considered in Fig. 6 is in fact the spectral efficiency $\Psi_{\max}(M)$ that minimizes the power dissipation. At high $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0$, it equals $\log_2(M^2)$, which is the maximum output entropy of the channel. This delivers a power dissipation of $\mathcal{P}_{\mathrm{ADC,\,min}} = \mathcal{P}_{\mathrm{ADC,\,min}} \cdot M^2/(\log_2(M^2))^{\nu}$.

The sample-and-hold capacitor noise limit indicates that 1-bit quantization at the receiver will be optimal to maximize the energy-efficiency at medium to high $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0$. In contrast, the power dissipation of state-of-the-art A/D converters suggests that 3-level quantization would be optimal. Note, however, that the power savings are only on the order of 10 % as compared to 1-bit quantization. The merits of 1-bit quantization are that a gain control can be omitted at the receiver, and that the optimal channel inputs are very simple and always the same (4-QAM with equally probable symbols), irrespective of the channel attenuation and noise. Therefore, 1-bit quantization might still be preferrable even if the data conversion at the receiver is 10 % less energy-efficient.

### C. Example

This example considers the design of a 60 GHz short-range system that achieves a throughput of 5 Gbit/s, as described in [20]. The system uses 4-QAM with analog phase equalization and 1-bit A/D conversion at the receiver. Considering the link budget, it can be shown that this system configuration is optimal for an energy-efficient receiver.

The available transmit power is 10 dBm. The channel attenuation is 55 dB at a distance of 2 m, which results in a received signal power of $-45$ dBm. The noise level, which includes a receiver noise figure of 10 dB, is $-165$ dBm. It follows that

$$\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0 = (120 - 10 \cdot \log_{10}(\Xi))\,\mathrm{dB} \tag{15}$$

A target throughput of 1 Gbps yields $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0 = 30\,\mathrm{dB}$, while a throughput of 5 Gbps delivers $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0 = 23\,\mathrm{dB}$. For both cases it is most energy-efficient to use 1-bit A/D converters (or alternatively A/D converters with 3 quantization levels, but with no more than 10 % additional energy savings), which can be seen from Fig. 6. The received signal power can even decrease to $-55$ dBm or $-62$ dBm, respectively, to yield $\mathcal{E}_{\mathrm{bit}}/\mathcal{N}_0 = 10\,\mathrm{dB}$, which still achieves the same throughput with the same A/D converter parametrization and power dissipation.

## VI. Summary And Conclusions

This work has analyzed the optimal parametrization of A/D converters in wideband communications receivers to minimize the energy consumption for a target system throughput. The focus has been on LOS channels without multi-path propagation, covering typical application scenarios such as wireless data kiosks or wireless chip-to-chip links in computer racks [21].

The analysis builds on a numerical computation of the exact channel capacity to calculate the minimum power dissipation as a function of the anticipated throughput for different channel conditions. State-of-the-art A/D converters have been surveyed to obtain an empirical expression for the power dissipation of todays designs in addition to the fundamental sample-and-hold capacitor noise limit.

The principle outcome of the analysis is the following: For the design energy-efficient wideband receivers, where the received signal power is sufficiently high as compared to the noise, it is optimal to use 1-bit A/D converters and scale the sampling rate with the target system throughput. The optimal modulation format is then 4-QAM. That is, system designs with large bandwidth but low spectral efficiency should be preferred. Only when the received signal power is close to the fundamental minimum that is required for error-free data transmission ($\gamma = -1.59\,\mathrm{dB}$), it becomes energy-efficient to use a higher quantization resolution.

Future work should extend the analysis to channels that are affected by multi-path propagation to cover further application scenarios such as wideband wireless local area networks. Another reasonable extension is to include a bandwidth constraint that accounts for frequency regulations in practice. It can be expected that higher quantization resolution is then more favorable. This reduces the energy efficiency.

## Acknowledgments

This work has been supported in part by the German Academic Exchange Service and by the German Federal Ministry of Education and Research under grant 01BU0813. The first author would like to thank Prof. U. Madhow (UC Santa Barbara) and J. Singh (Samsung Telecommunications America) for the valuable introduction to the Cutting-Plane algorithm, and Behnam Sedighi (IHP Microelectronics) for the discussion on the power dissipation of modern A/D converters.

## References

[1] J. Singh *et al.*, "On the Limits of Communication with Low-Precision Analog-to-Digital Conversion at the Receiver," *IEEE Transactions on Communications*, vol. 57, no. 12, 2009.

[2] A. Mezghani and J. A. Nossek, "How to Choose the ADC Resolution for Short-Range Low Power Communications," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'10)*, 2010.

[3] R. G. Gallager, *Information Theory and Reliable Commuunication*. John Wiley & Sons, Inc., 1968.

[4] J. Huang and S. P. Meyn, "Characterization and Computation of Optimal Distributions for Channel Coding," *IEEE Transactions on Information Theory*, vol. 51, no. 7, 2005.

[5] B. Le *et al.*, "Analog-to-Digital Converters," *IEEE Signal Processing Magazine*, vol. 22, no. 6, 2005.

[6] T. Sundstroem *et al.*, "Power Dissipation Bounds for High-Speed Nyquist Analog-to-Digital Converters," *IEEE Transactions on Circuits and Systems - I: Regular Papers*, vol. 56, no. 3, 2009.

[7] P. B. Kenington and L. Astier, "Power Consumption of A/D Converters for Software Radio Applications," *IEEE Transactions on Vehicular Technology*, vol. 49, no. 2, 2000.

[8] B. Murmann, "*ADC Performance Survey 1997 - 2010*," [Online]. Available: http:// www.stanford.edu/∼murmann/adcsurvey.html, 2010.

[9] P. Nuzzo *et al.*, "A 10.6mW/0.8pJ power-scalable 1GS/s 4b ADC in 0.18$\mu$m CMOS with 5.8GHz ERBW," *Proc. of the Annual Design Automation Conference*, 2006.

[10] I.-H. Wang and S.-I. Liu;, "A 1V 5-Bit 5GSample/sec CMOS ADC for UWB Receivers," *International Symposium on VLSI Design, Automation and Test (VLSI-DAT 2007)*, 2007.

[11] M. Choi *et al.*, "A 6-bit 5-GSample/s Nyquist A/D converter in 65nm CMOS," *Proc. of the IEEE Symp. on VLSI Circuits (VLSI'08)*, 2008.

[12] H.-G. Wei *et al.*, "A Power Scalable 6-bit 1.2GS/s Flash ADC with Power on/off Track-and-Hold and Preamplifier," *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS'08)*, 2008.

[13] H. Yu and M.-C. F. Chang, "A 1-V 1.25-GS/S 8-Bit Self-Calibrated Flash ADC in 90-nm Digital CMOS," *IEEE Transactions on Circuits and Systems - II: Express Briefs*, vol. 55, no. 7, 2008.

[14] R. A. Kertis *et al.*, "A 35 GS/s 5-Bit SiGe BiCMOS Flash ADC with Offset Corrected Exclusive-Or Comparator," *Proc. of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM'08)*, 2008.

[15] D. Ferenci *et al.*, "Design of a 3 Bit 20 GS/s ADC in 65 nm CMOS," *International Conference on Ph.D. Research in Microelectronics and Electronic (PRIME'09)*, 2009.

[16] P. Veldhorst *et al.*, "A 0.45pJ/conv-step 1.2Gs/s 6b Full-Nyquist Non-Calibrated Flash ADC in 45nm CMOS and Its Scaling Behavior," *Proc. of the European Solid-State Circuits Conference (ESSCIRC '09)*, 2009.

[17] J. Yang *et al.*, "A 1-GS/s 6-bit 6.7-mW ADC in 65-nm CMOS," *Proc. of the Custom Intergrated Circuits Conference (CICC'09)*, 2009.

[18] Y. Nakajima *et al.*, "A Background Self-Calibrated 6b 2.7 GS/s ADC With Cascade-Calibrated Folding-Interpolating Architecture," *IEEE Jurnal of Solid-State Circuits*, vol. 45, no. 4, 2010.

[19] D. Tse and P. Viswanath, *Fundamentals of Wireless Communications*. Cambridge University Press, 2005.

[20] S. Krone *et al.*, "Physical Layer Design, Link Budget Analysis and Digital Baseband Implementation for 60 GHz Short-Range Applications," *EuMA International Journal of Microwave and Wireless Technologies.*, vol. 3, no. 2, 2011.

[21] G. Fettweis, F. Guderian, and S. Krone, "Entering the Path Towards Terabit/s Wireless Links," *Proceedings of the Design, Automation, and Test in Europe Conference (DATE'11)*, 2011.